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FIG. 3A through 3C are respectively a plan view illustrating a unit chip region of a wafer on which a reference layer pattern has been defined using the reference-layer-defining photomask, a cross-sectional view illustrating an on-wafer intended pattern region and a cross-sectional view illustrating an on-wafer alignment region in accordance with the first embodiment.

A second inventive alignment method includes the step of a) preparing a reference-layer-defining photomask on which a first on-mask alignment accuracy measuring mark and an on-mask alignment mark have been formed. The first on-mask alignment accuracy measuring mark has a size equal to that of a first on-wafer intended pattern for a reference layer. The on-mask alignment mark has a size equal to that of a second on-wafer intended pattern to be defined in a layer-to-be-aligned. The method further includes the step of b) preparing a layer-to-be-aligned-defining photomask that includes at least a second on-mask intended pattern for defining the second on-wafer intended pattern in the layer-to-be-aligned. The method further includes the step of c) forming the first on-wafer intended pattern and an on-wafer alignment accuracy measuring mark on a wafer by using the reference-layer-defining photomask. The on-wafer alignment accuracy measuring mark is formed by transferring the on-mask alignment accuracy measuring mark. And the method further includes the step of d) aligning the layer-to-be-aligned-defining photomask by reference to the position of the on-wafer alignment accuracy measuring mark for the reference layer.

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FIGS. 3A through 3C are respectively a plan view illustrating a unit chip region of a wafer on which a reference layer pattern has been defined using the reference-layer-defining photomask, a cross-sectional view illustrating an on-wafer intended pattern region and a cross-sectional view illustrating an on-wafer alignment region in accordance with the first embodiment.

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FIGS. 3A through 3C are respectively a plan view illustrating a unit chip region of a wafer on which a reference layer pattern has been defined using the reference-layer-defining photomask shown in FIGS. 1A through 1D, a cross-sectional view illustrating an on-wafer intended pattern region and a cross-sectional view illustrating an on-wafer alignment region. As shown in FIG. 3A, the unit chip region **Rtpwf** includes the on-wafer intended pattern region **21**,

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on-wafer alignment accuracy measuring regions **22**, and first and second on-wafer alignment regions **23x** and **23y**. An isolation film pattern for transistors to be fabricated in the chip has been defined in the on-wafer intended pattern region **21**. Each of the on-wafer alignment accuracy measuring regions **22** includes an alignment accuracy measuring mark for measuring the alignment accuracy. The first and second on-wafer alignment regions **23x** and **23y** include alignment marks that are necessary for the alignment with a layer-to-be-aligned pattern.

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Next, before the layer-to-be-aligned pattern is formed over the wafer using the layer-to-be-aligned-defining photo-mask shown in FIGS. **4A** through **4C**, a shift Δx between the actual and ideal distances between any pair of on-wafer alignment marks **33a** and **33b** of the first and second groups is measured. The ideal distance is stored in a database for the stepper. The shift Δx is used as a correction for the next alignment step for forming the layer-to-be-aligned pattern.

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As also shown in FIG. **5B**, the on-wafer intended pattern **32** (first on-wafer intended pattern) has already been defined for the reference layer by the isolation film **31** and wafer surface in the on-wafer intended pattern region **71**. A gate resist pattern **83** is going to be formed so that a gate pattern **84** (second on-wafer intended pattern) will be made up of multiple gate electrodes arranged three by three at a width of $0.5\ \mu\text{m}$ and a space of $0.5\ \mu\text{m}$ through a patterned process for the layer-to-be-aligned. As shown in FIG. **5C**, the poly silicon film **81** and the photoresist film **82** are also formed on the first and second groups of on-wafer alignment marks **33a** and **33b** for the reference layer, which have been formed in the process step shown in FIGS. **3A** through **3C**. However, no alignment marks will be newly formed in this region, and no pattern will be defined in this part of the photoresist film.
